Dkt: 884.A53US1 (INTEL)

Title: SYSTEM AND METHOD FOR CHANNELIZATION RECOGNITION IN A WIDEBAND COMMUNICATION SYSTEM

Assignee: Intel Corporation

IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 2, line 13 is amended as follows:

FIG. 7 FIGs. 7A, 7B, 7C and 7D illustrates filter response of matched filters in accordance with some embodiments of the present invention; and

The paragraph beginning at page 12, line 16 is amended as follows:

FIG. 7 illustrates FIGs. 7A, 7B, 7C and 7D illustrate filter responses of matched filters in accordance with some embodiments of the present invention. Filter responses 702 through 708 may illustrate the filter responses over time for four matched filters, such as filters 206 (FIG. 2), when used as part of circuitry 200 (FIG. 2) for generating a channelization vector, such as channelization vector 208 (FIG. 2). FIG. 7 illustrates FIGs. 7A, 7B, 7C and 7D illustrate the generation of channelization vector "1001". Filter response 702 (FIG. 7A) of a first matched filter is illustrated as exceeded threshold 712 which may provide a "1" in the first position of the channelization vector. Filter response 704 (FIG. 7B) is illustrated as not exceeding threshold 712 which may provide a "0" in the second position of the channelization vector. Filter response 706 (FIG. 7C) is illustrated as not exceeding threshold 712 which may provide a "0" in the third position of the channelization vector. Filter response 708 (FIG. 7D) is illustrated as exceeding threshold 712 which may provide a "1" in the fourth position of the channelization vector. The generation of channelization vector "1001" may indicate that the first and fourth subchannels are active and that the second and third subchannels are inactive.